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Electromigration in Integrated Circuits: Nano-Scale Processes Affecting the Reliability of Kilometers of Wiring

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Summary

Modern high-performance ICs have several *kilometers* of wiring per square centimeter of circuit. This wiring consists of Cu-filled trenches in up to 12 stacked layers of insulating SiO2-based materials. These Cu wires have widths as low as 130nm and the trenches must be lined with refractory metal diffusion barriers that are only 5nm thick. Further dimensional scaling to accommodate Moore's law (a doubling of devices per IC every 18 months) requires that the length of interconnect per IC increase at an exponential rate, and that the width of the Cu wires and refractory metal liners decrease at an exponential rate. At the same time, these Cu wires must carry currents (as high as 2 x 106A/cm2 in current ICs) that must also increase at an exponential rate. This evolution poses serious concerns about the ability to produce future ICs with reliable interconnects.

Electromigration, current-induced mass transport, is the chief reliability concern for future IC interconnects. Electromigration is the result of momentum transfer from conducting electrons to metal atoms that cause the atoms to diffuse in the direction of electron flow. Electromigrating atoms accumulate and or lead to mass depletion at sites where there atomic flux diverges. Accumulation of copper leads to compressive stresses that can causes extrusions and lead to short circuit failures, and depletion of copper leads to tensile stresses that can cause nucleation and growth of voids that cause open circuit failures. The magnitudes of the stresses that develop depend on the current density, the distance between flux divergence sites, and the elastic response of the material that surrounds the copper. The magnitude of the stresses that will cause failure depends on adhesion at the interfaces between copper and the surrounding materials.

Accurate assessment of the circuit-level reliability of interconnect structures requires modeling of different types, focusing on phenomena that occur at multiple length scales. In past work, we have developed models for circuit-level reliability assessments that are based on experimental characterization and modeling of electromigration-induced failure of *interconnect trees*, which can be treated as independent reliability units. This has allowed development of layout-specific tools for reliability assessment, accounting for the reliability of the millions of different interconnect trees that constitute an IC interconnect system.

More recent work has focused on in-situ experimental observations of void nucleation, drift, and accumulation in interconnect segments. We have investigated

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the effects of Cu grain structures and crystallographic orientations on void nucleation, growth, and drift, and have developed simple simulations and analytic models for these processes. These models suggest that the dynamic nature of voiding in interconnects require reconsideration of standard assumptions and treatments for assessment of circuit-level reliability. The recognition of the important role of dynamic void interactions also calls for modified interconnect design and layout strategies.